A 'A

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/804,523	03/12/2001	Michael T. Moore	0325.00361	9089

21363 7590 05/15/2003

CHRISTOPHER P. MAIORANA, P.C.
24025 GREATER MACK
SUITE 200
ST. CLAIR SHORES, MI 48080

EXAMINER
TRAN, ANH Q

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 05/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

A - A

Office Action Summary	Application No.	Applicant(s)	
	09/804,523	MOORE, MICHAEL T.	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 15-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 15-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, 7-13, 15-24 are rejected under 35 U.S.C. 102(b) as being anticipated by New (5,874,834).

Regarding claim 1, New shows an apparatus (Fig. 2-8) comprising:

One or more logic circuits (Fig. 6A) configured to provide logical operation, wherein the one or more logic circuits comprise (i) programmable logic elements (CLE) and (ii) non-programmable logic elements (SOG) within a programmable logic device, wherein the programmable logic elements are (i) configurable between two or more different logical functions (col. 4, lines 65-col. 5, line 7) and (ii) connectable by a routable interconnect circuit (switch matrix).

Regarding claim 2, New shows the one or more logic circuits comprise variable width logic circuit (col. 3, lines 62-66).

Regarding claims 3-4, New shows a width of each of the one or more logic circuits is determined in response to one or more input signals, wherein the inputs comprise multi-bit or single-bit signals in a serial or a parallel configuration (col. 4, lines 25-64).

Regarding claim 5, New shows wherein one or more of the logic circuits comprises a hard wired multiplier (col. 5, lines 3-36).

Regarding claims 7-8, New shows each of the one or more outputs comprise intermediate signals.

Regarding claim 9, New shows an adder (col. 5, line 4) configured to receive the one or more outputs (example, one of CLB '200C' as one logic circuit with the outputs and CLB '200' with the CLE 202 configured as an adder).

Regarding claim 10, New shows the routable interconnect circuit is configured to route signals to/from one or more of the non-programmable elements.

Regarding claims 11, New shows further comprising a number of registers configured to increase a throughput of the one or more logic circuits (304 & 305, Fig. 5).

Regarding claims 12-13, New shows each of the one or more logic circuits comprises an input portion configured to store input signals and an output portion configured to store an output (one CLB can be configured as input storage circuit to one of the CLB and other CLB can be configured as an output storage circuit, all three circuit connected as one circuit).

Claims 15-22 are rejected as above.

Regarding claim 23, New shows one or more first registers (304 & 305, Fig. 5) configured to coupled one or more input signals to the non-programmable logic elements (304 & 305 of 202B of Fig. 3 coupled the input signals to the SOG 203B); and one or more second registers (304 & 305 of 202A) configured to receive one or more output signals from the non-programmable logic elements.

Regarding claim 23, New shows the non-programmable logic elements (SOG, Fig. 3) comprise hard wired multipliers (col. 5, line 3) having a first width (inherent limitation since all circuit have width) and are couplable to form one or more multipliers having a second width (Fig. 3 shows that the SOGs are couplable together to form larger or wider width).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over New in view of applicant's prior art on page 2-3.

New discloses the claimed invention except for teaching one or more logic circuits are configured to perform a cyclic redundancy check functions. Applicant's prior art teaches a CPLDs and FPGAs are frequently used to implement cyclic redundancy check functions. Therefore, it would obvious to one having ordinary skill in the art at the time the invention was made to configure the FPGA of New for cyclic redundancy check functions for error checking.

Response to Arguments

5. Applicant's arguments filed 2/24/03 have been fully considered but they are not persuasive. Applicant argue that "New does not disclose or suggest non programmable logic elements, as presently claimed". However, New discloses the SOG gate array is non-field programmable gate array which is mask programmed gate array (col. 1, lines 50-52). Mask programmed gate is configured during manufacture stages only, once an mask programmed gate has been designed and manufactured it cannot be reconfigured to perform a different function. **The circuit in the mask programmed gate are hard wired connections**. The term "mask programmed" is well known in the art which referred to an application specific integrated circuit as hard wired connection circuit. The reference, Lien et al (6,211,697), which was provided to Applicant in the previous office action for better understanding the term "**mask programmed**". Lien discloses once an ASIC has been designed and manufactured it cannot be reconfigured to perform a different function like the FPGA can. Similar to an ASIC, a "hard" gate array (GA), i.e., a non-programmable GA, can be designed to perform a specific function. Such a GA will also be smaller than an FPGA that has been programmed to perform that same specific function due to the elimination of excess circuitry. Furthermore, a GA is more likely to be a faster device and less power consuming than an FPGA. This is because many of the circuit connections within the FPGA are provided by transistors, whereas **circuit connections in the GA are hard wired connections** (col. 2, lines 50-64). In column 4, lines 40-62, Lien discloses **the hard gate array (HA) is a mask metal programmable gate array** which is programmed during IC chip manufacturing process. In general,

much of excess circuitry (e.g., programmable switches and corresponding memories) of the FPGA has been eliminated in the HA. In column 5, lines 11-15, The implementation of the HA is done in factory, preferably using the top layer mask or a near top layer mask to deposit metal connections to selected areas, as dictated by the configuration data provided by the companion design software.

Therefore, New mask-programmable gate array (SOG) is non-programmable logic elements.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 703-306-4507. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 703-305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7724 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Anh Tran
May 6, 2003